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EXAMINER	
TRUJILLO, JAMES K	

ART UNIT	PAPER NUMBER
2116	6

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/672,395	CHENG ET AL.	
	Examiner	Art Unit	
	James K. Trujillo	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The office acknowledges the receipt of the following and placed of record in the file: Amendment A and Declaration both dated 1/20/04.

2. Claims 1-21 are presented for examination.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Applicant's arguments with respect to claim 1-20 have been considered but are moot in view of the new ground(s) of rejection.

5. Claims 1-2, 6-13, 16-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Jr., U.S. Patent 5,630,110 (hereinafter Mote) in view of Pole, II et al., U.S. Patent 6,311,281 (cited in last office action, hereinafter Pole) and Applicant's admitted prior art (hereinafter AAPA).

6. As to claim 1, Mote substantially teaches, as per claim 1, an apparatus comprising a circuit configured to:

a. change a frequency of one or more first signals (operating speed of the CPU) in response to a second signal (causing a change in frequency) [col. 5 lines 26-30 and col. 31-36].

Mote does not expressly disclose generating a third signal in response to either said second signal or a predetermined time expiring.

Pole teaches an apparatus that generates a third signal (reset for a processor) in response to another signal (change of frequency) [col. 2 lines 16-21].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mote by generating the third signal (the reset) in response to the second signal (to cause the change in frequency) as taught by Pole because all systems are directed toward changing the frequency of a processor. An artisan would have been motivated to make the modification because Pole teaches that resetting the processor is necessary for the desired on-the-fly change of frequency that allows for a desired quick change in performance level [col. 2 lines 16-34]. These features are also desirable in Mote.

AAPA teaches that if the frequency of a programmable clock circuit changes faster than the microprocessor can track the microprocessor will hang. AAPA further teaches a conventional apparatus used in recovering a system from a failure, such as a hang, by generating a third signal (a reset for resetting the microprocessor) in response to a predetermined time period expiring using a watchdog timer in the case of a hang [page 2 line 1 through page 3 line 2].

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote combined with Pole by incorporating the apparatus taught by AAPA to recover from a failure because both systems are directed toward recovering a system from a failure. The modification would be made by adding a watchdog timer using a predetermined time period to reset the microprocessor of Mote when a failure occurs as taught by AAPA. The reset would occur with the frequency prior to the failure. An artisan would have been motivated to make the modification because the modification would ensure that the system of Mote would

continue repeat the steps of adjusting the frequency especially the failure which occurred hangs the system.

7. As to claim 2, Mote together with Pole and AAPA taught the apparatus according to claim 1 described above. Mote further suggests that the second signal may be used to program (using successive approximation methods automatically) the first signal to change its frequency [col. 6 lines 36-39].

8. As to claim 6, Mote combined with Pole and AAPA taught the apparatus according to claim 1 described above. AAPA further taught wherein the predetermined time period is programmable. AAPA uses a watchdog timer to reset after a preset amount of time, which implicitly teaches that the time period would be programmable. Alternatively, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mote combined with AAPA an Pole by using a programmable watchdog timer because they are well known and widely used in the computer art to reset a processor. An artisan would have been motivated to make such a modification because it is desirable to make the system flexible with respect to the amount of time before a reset is issued.

9. As to claim 7, Mote combined with Pole and AAPA taught the apparatus according to claim 1 described above. Mote combined with Pole and AAPA together do not expressly disclose wherein said predetermined time period is started in response to said second signal. However, Pole teaches that a third (reset) signal should be issued when changing the frequency (a second signal) of the system. AAPA teaches using a predetermined time period to recovery from a system hang by issuing a third (reset) signal.

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote combined with Pole and AAPA by starting the predetermined time period (as taught by AAPA) in response to the second signal (frequency adjustment), because it is desirable to reset the processor when changing the frequency as set forth hereinabove by Pole. However, an artisan would recognize that if the frequency of adjustment were such that the processor hangs, as AAPA suggests teaches, there would be no automatic recovery, forcing user intervention. Therefore, making the modification would allow an automatic recovery (from a hang) to be enabled, desirably reducing the need for user intervention, when the predetermined time period is initiated in response to the second signal.

10. As to claim 8, Mote together with Pole and AAPA taught the apparatus according to claim 1 described above. AAPA further taught using a watchdog timer circuit that measures the predetermined time period [figure 1].

11. As to claim 9, Mote together with Pole and AAPA taught the apparatus according to claim 1 described above. Mote further teaches wherein one of the first signals is presented to a clock input of a processor because Mote discloses that his invention is directed toward adjusting the clock control settings at different operating frequency for a processor [abstract]. It is inherent that adjusting different operating frequencies entails changing the clock input of a processor.

AAPA teaches wherein of the third signal would be presented to a reset input of said processor [figure 1].

12. As to claim 10, Mote together with Pole and AAPA taught the apparatus according to claim 9 described above. Mote together with Pole and AAPA do not expressly disclose wherein said second signal is generated using a number of instructions executed by said processor.

However, Mote teaches that the clock rate is controlled digitally [col. 2 lines 8-19]. Mote also teaches that the performance could be implement by a PC owner. Therefore, it would have been obvious to one of ordinary to further modify Mote together with Pole and AAPA by generating the second signal using instructions executed by the processor because it would make it easier for an owner to enhance the system.

13. As to claim 11, Mote together with Pole and AAPA taught the apparatus according to claim 10 described above. The instructions as set forth hereinabove would be used by a processor and therefore must be contained in a computer readable medium.

14. As to claim 12, Mote combined with Pole and AAPA taught the apparatus according to claim 10 described above. Mote combined with Pole and AAPA do not expressly disclose wherein said instructions are part of a basic input output system routine. However, one of ordinary skill in the art will readily recognize that the adjustment of the frequency would desirably take place prior to the normal operation of the computer. It is well known in the computer arts prior to the normal operation a computer system uses the basic input output system routine to operate and set parameters. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify the combination of Mote combined with Pole and AAPA by implementing the instructions as part of a basic input output system routine because it would enable the frequency to be adjusted prior to the normal computer operation.

15. As to claim 13, Mote combined with Pole and AAPA taught the apparatus according to claim 9 described above. Mote combined with Pole and AAPA do not expressly disclose wherein the predetermined time period expires only when the processor hangs. It is well known in the computer arts that watchdog timers use a predetermined time period that expires only

when the processor hangs. AAPA teaches using a watchdog timer to reset a processor. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote combined with Pole and AAPA by requiring the predetermined time period of the watchdog timer to expire only when the processor hangs.

16. As to claims 16 and 17, Mote combined with Pole and AAPA taught the apparatus according to claim 1 described above. Mote combined with Pole and AAPA does not expressly disclose wherein said circuit is configured to skew said one or more first signals.

However, Mote discloses that one or more first signals are distributed to different logic and memory circuits using different paths. An artisan would have recognized that in distributing the one or more first signals through different paths would require skew times to be adjusted for each path accordingly to ensure proper clocking of the system. Having programmable skew in data and clock signal paths is well known in the computer arts to ensure proper clocking of the system.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mote combined with Pole and AAPA by having a circuit configured to skew said one or more first signal by incorporating programmable skew or delay for each particular signal path. An artisan would have been motivated to make such a modification to ensure proper timing throughout the system ensuring data is transferred correctly.

17. As to claim 18, claim 18 is rejected for the same reasons as set forth hereinabove.

18. As to claim 19, Mote combined with Pole and AAPA taught the claimed apparatus therefore together they teach the claimed method to operate the claimed apparatus.

19. As to claim 20, Mote combined with Pole and AAPA taught the claimed method according to claim 19 described above. Mote further teaches wherein when the processor hangs, changing said frequency of said clock signal to a fail-safe frequency [figure 3] and Pole teaches resetting said processor.

In summary, Mote teaches changing the frequency to obtain a desired timing margin and desired frequency of said clock. In changing the frequency Mote increases the frequency until failure. If a failure occurs, Mote then sets the frequency and sets clock control settings to a different clock setting. Pole teaches that after changing the frequency a reset is necessary.

20. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Pole and AAPA in further view of Tanoi, U.S. Patent 5,751,665 (cited in last office action, herein after "Tanoi").

21. As to claim 3, Mote together with Pole and AAPA taught the apparatus according to claim 1 described above. Mote teaches one first signal generated by one phase lock loop circuit [figure 2]. Mote does not expressly disclose wherein more than one first signals are generated by more than one phase lock loop circuits.

Tanoi teaches using more than one phase lock loop circuits to generate more than one first signal [figure 14].

It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote together with Pole and AAPA by incorporating more than one phase lock loop circuits as taught by Tanoi because both invention are directed toward clocks in

microprocessors. One of ordinary skill would have made the modification because Tanoi teaches that clock skew can be reduced, which would be desirable in Mote.

22. As to claim 4, Mote together with Pole, AAPA and Tanoi taught the apparatus according to claim 3 described above. Mote together with Pole, AAPA and Tanoi do not expressly disclose wherein the second signal programs said one or more phase lock loop circuits. However, one of ordinary skill would have reasoned that the second signal should be used to program all of the phase lock loop circuits to achieve the desired result of obtaining an optimum frequency for the system. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote together with Pole, AAPA and Tanoi by programming all of the phase lock loops according to the second signal.

23. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Pole and AAPA as applied to claim 1 above, and further in view of Ogilvie et al., U.S. Patent 6,038,629 (cite in previous office action, hereinafter Ogilvie).

24. As to claim 5, Mote combined with Pole and AAPA taught the apparatus according to claim 1 described above. However, Mote combined with Pole and AAPA do not expressly teach wherein said one or more first signals are generated using a divider network. Specifically, Mote teaches that clock signals are distributed to various logic, processor, and memory circuits. Mote is silent with respect to how the clock signals are distributed.

Ogilvie taught an apparatus having one or more phase lock loops wherein the clock signals of one of the phase lock loops is distributed using a divider network to provide clock signals to various logic, processor and memory circuits [col. 8 lines 10-17].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination of Mote, Pole and AAPA by using a divider network as taught by Ogilvie because all necessary systems are directed toward distributing clock signals. An artisan would have been motivated to make the modification because the divider network as taught by Ogilvie would allow different clock frequencies to be distributed, which would be desirable in the combination of Mote, Pole and AAPA.

25. Claims 14 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Pole and AAPA in further view of Finch et al., U.S. Patent 5,513,319.

26. As to claims 14 and 21, Mote together with Pole and AAPA taught the apparatus according to claim 1 described above. AAPA, as set forth hereinabove, further taught wherein the third signal is configured to reset a processor. Mote together with Pole and AAPA does not expressly teach wherein said circuit is configured to generate a fourth signal in response to the expiration of said predetermined time period and wherein said fourth signal is configured to reset an entire system.

Finch teaches that a third signal that is reset signal is sent to a processor (CPU). In Finch if the processor is locked and cannot respond the entire system (PC system) is reset (restarted) using a fourth signal [col. 5 lines 53-65].

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Mote together with Pole and AAPA with the teachings of the fourth signal as an entire system reset as taught by Finch because all system are directed toward computer systems. One of ordinary skill would have made the modification because Finch teaches that doing so would

desirably restart the system without user intervention and would provide a means to identify the cause of the malfunction [col. 2 lines 36-41].

27. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mote, Pole and AAPA as applied to claim 1 above, and further in view of I^2C Bus specification (submitted in IDS, hereinafter "the I^2C Bus specification").

28. As to claim 15, Mote combined with Pole and AAPA taught the apparatus according to claim 1 described above. Mote combined with Pole and AAPA do not expressly wherein said circuit comprises an inter-integrated circuit interface circuit.

The I^2C Bus specification teaches using an I^2C Bus has many advantages [pages 4-6]. It would have been obvious to one of ordinary skill in the art at the time of the invention to further modify Mote combined with Pole and AAPA incorporating within their circuitry an inter-integrated (I^2C) interface circuit. An artisan would have made the modification because the I^2C Bus specification teaches that it is beneficial to use an I^2C bus for coordinating data and clock signals between buses. In using an I^2C Bus, an inter-integrated (I^2C) interface circuit would be necessary, resulting in the claimed invention.

Conclusion

29. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

> U.S. Pat. No. 6,014,033 to Fitzgerald et al. This patent teaches adjusting the clock frequency of an integrated circuit to determine the operating parameters.

U.S. Pat. No. 6,385,735 to Wilson et al. This patent teaches adjusting the frequency of processor up to a limit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to James K. Trujillo whose telephone number is (703) 308-6291. The examiner can normally be reached on M-F (7:30 am - 5:00 pm) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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James Trujillo
March 10, 2004

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